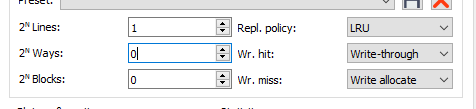
# Experiment 10: Cache Visualization and Simulation in Ripes

|  |  |  |
| --- | --- | --- |
| **Sl No** | **Name** | **ID No** |
| **1** | **Dhruv Makwana** | **2019A3PS0381H** |

The aim of this experiment is to understand the basic principles of different configurations of Cache with the help of Ripes tool. The tool assumes that the instruction and data cache are separate. You will be able to select different configurations of Cache (see the figure below for reference).

Indicates the number of Sets (1 indicates 21 Sets)



Indicates the number of words in the block (1 indicates 21words in a block)

Indicates the number of blocks in the set (1 indicates 21blocks in a set)

(The cache sizes are set to lower size for understanding purposes)

**Consider the following program (or any other program of your choice).**

.data

N: .word 0x0a

Value: .word 0x32, 0x20, 0x12, 0x45, 0x56, 0x21, 0x67, 0x10, 0x67, 0x90

.text

lw t0, N

la t1, Value

Loop:

lw s0, 0(t1)

lw s0, 0(t1)

addi t1, t1, 4

addi t0, t0, -1

bne t0, zero, Loop

**If you have used a different program, copy the image of the program below:**

**Answer:**

**Direct Mapped Single word and Multiword cache**

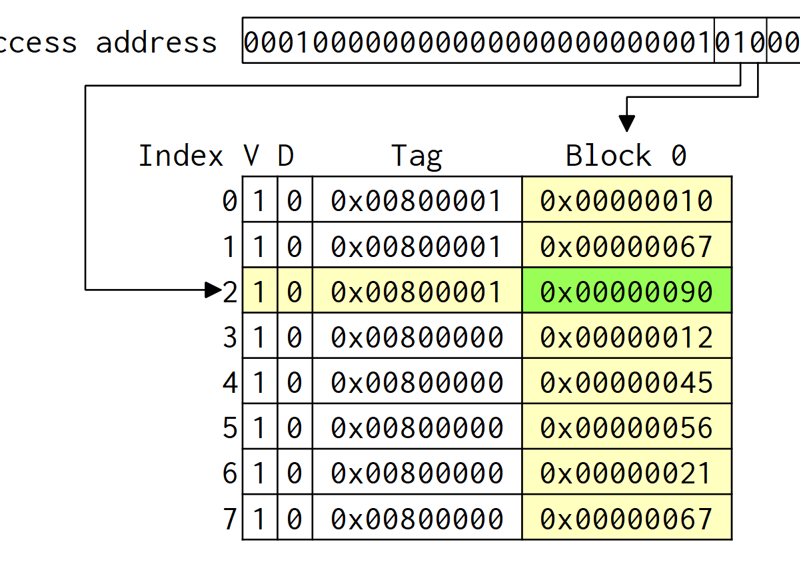
1. **Test the above program with the following configuration for data cache (observe the data cache access behavior)**

**Cache Type = Direct Mapped Cache**

**No of Blocks = 8**

**No of Words in the Block = 1**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: 

1. **What is the miss rate for data cache?**

Answer:0.5238

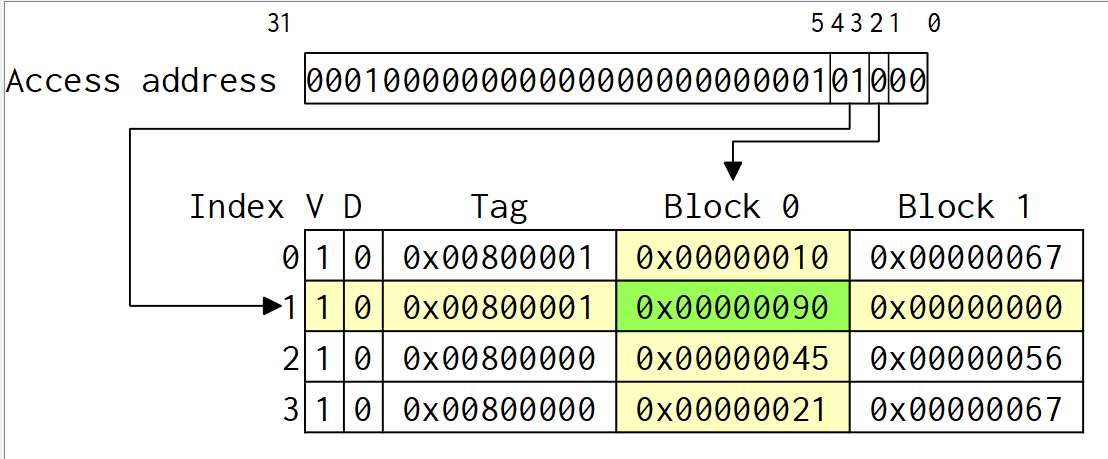
1. **Test the above program with the following configuration for data cache (observe the cache access behavior, specifically cache write)**

**Cache Type = Direct Mapped Cache**

**No of Blocks = 4**

**No of Words in the Block = 2**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: 

1. **What is the miss rate for data cache?**

Answer:0.2857

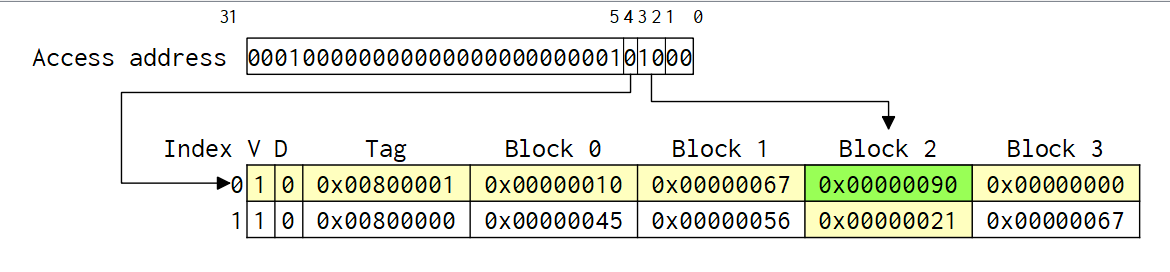
1. **Test the above program with the following configuration for data cache (observe the cache access behavior, specifically cache write)**

**Cache Type = Direct Mapped Cache**

**No of Blocks = 2**

**No of Words in the Block = 4**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: 

1. **What is the miss rate for data cache?**

Answer:0.1429

**Set-Associative Single word and Multiword cache**

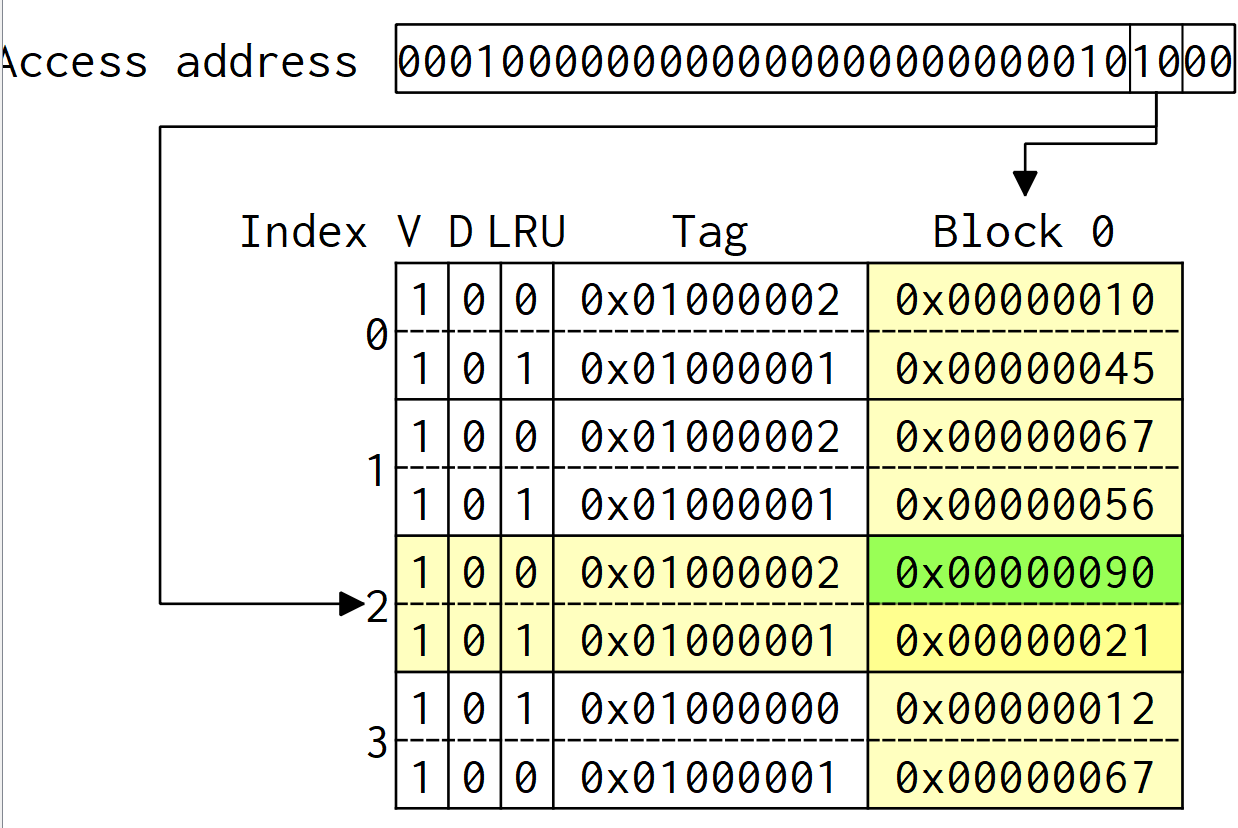
1. **Test the above program with the following configuration for data cache (observe the cache access behavior, specifically the implementation of LRU)**

**Cache Type = 2-way Set Associative (2 blocks per set)**

**No of Blocks = 8**

**No of Words in the Block = 1**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: 

1. **What is the miss rate for data cache?**

Answer: 0. 5238

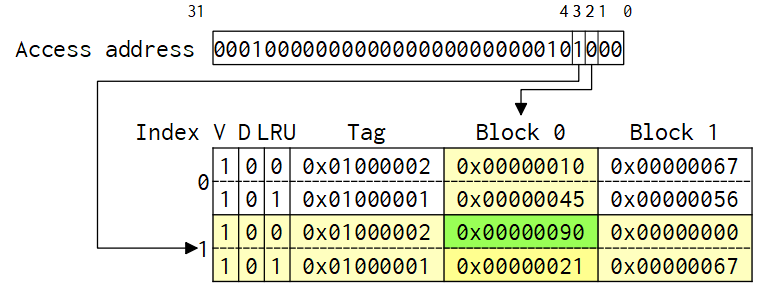
1. **Test the above program with the following configuration for data cache (observe the cache access behavior, specifically the implementation of LRU)**

**Cache Type = 2-way Set Associative (2 blocks per set)**

**No of Blocks = 4**

**No of Words in the Block = 2**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: 

1. **What is the miss rate for data cache?**

Answer: 0. 2857

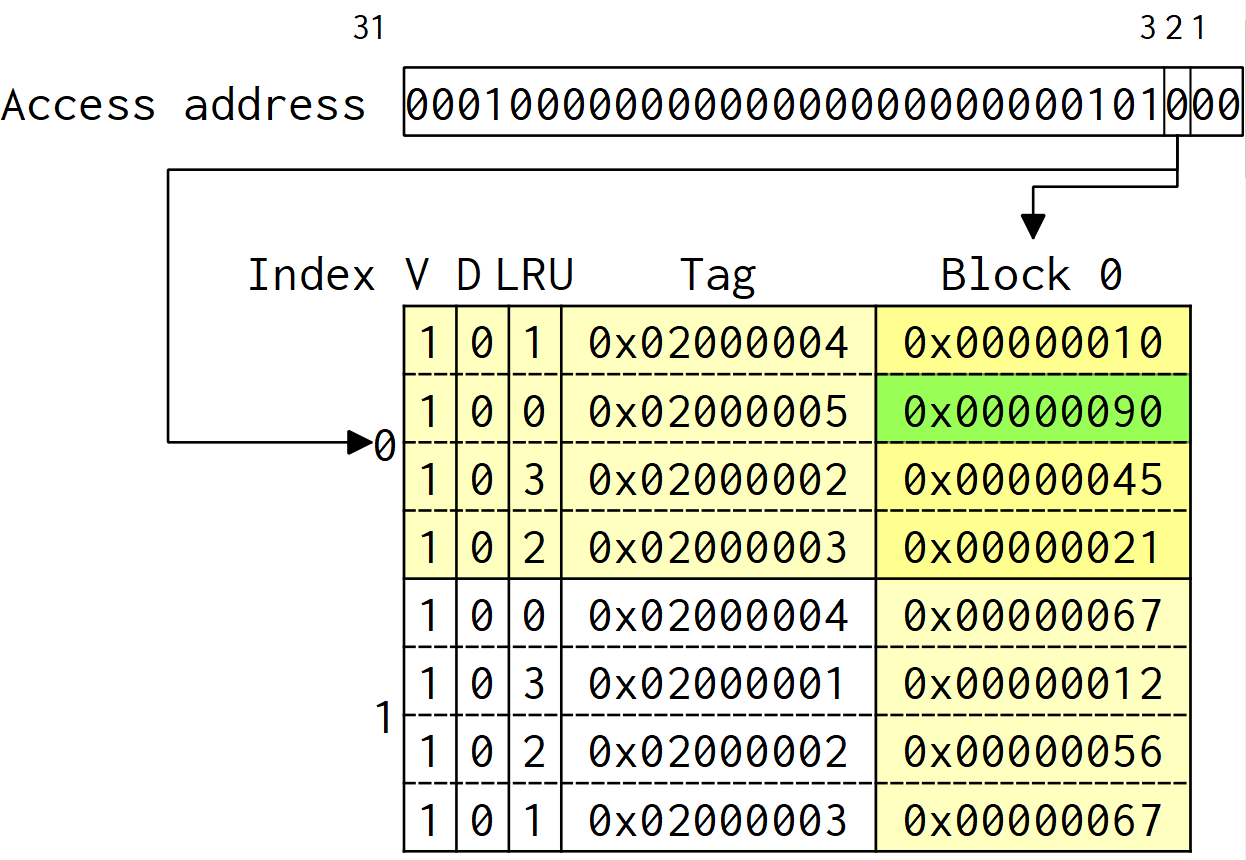
1. **Test the above program with the following configuration for data cache (observe the cache access behavior, specifically the implementation of LRU)**

**Cache Type = 4-way Set Associative (4 blocks per set)**

**No of Blocks = 8**

**No of Words in the Block = 1**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: 

1. **What is the miss rate for data cache?**

Answer: 0. 5238

1. **Test the above program with the following configuration for data cache (observe the cache access behavior, specifically the implementation of LRU)**

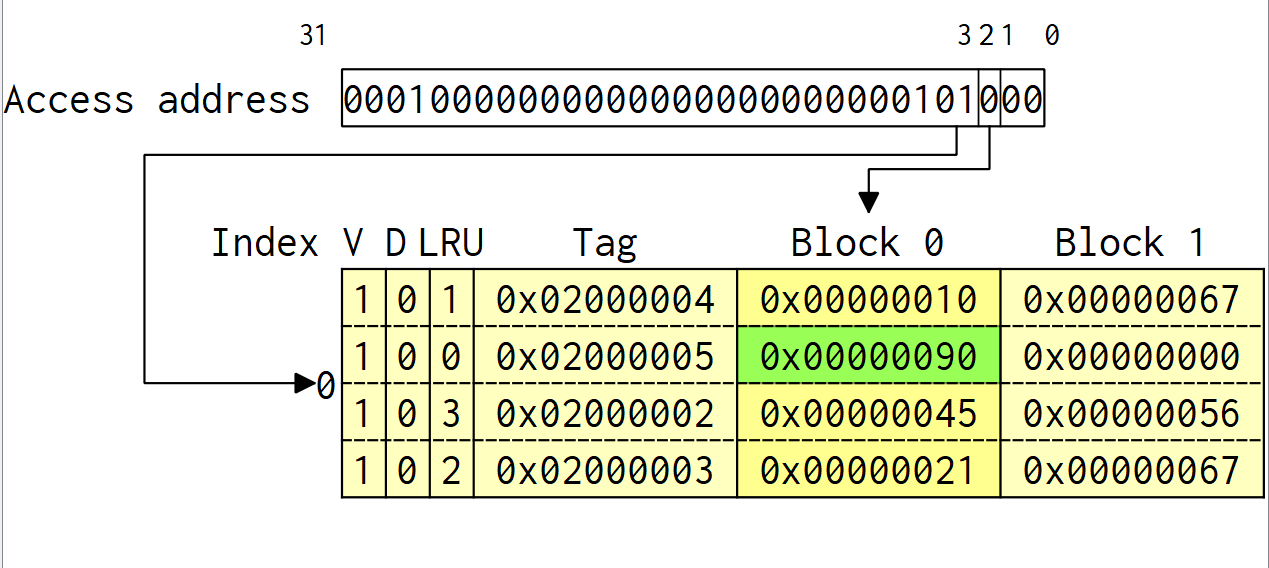
**Cache Type = 4-way Set Associative (4 blocks per set)**

**No of Blocks = 4**

**No of Words in the Block = 2**

**(Note this configuration is equivalent to fully associative cache)**

1. **Paste the image of final status of data cache after the execution of the above program.**

Answer: ****

1. **What is the miss rate for data cache?**

Answer: **0.**2857

1. **Explore other cache configurations and understand the cache behavior.**
2. **List the concepts you learnt from this experiment. (Conclusion/observations)**

Answer: We learned how cache works and the terms associated with it